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J.C.

(9) FINAL REPORT ON (6) FEASIBILITY STUDY FOR A THIN FILM MEMORY SYSTEM

(15) CONTRACT NO. Nobsr-87314

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(16) Task No. 7131

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Prepared for: Bureau of Ships
Department of the Navy
Washington 25, D. C.

Prepared by: CBS Laboratories, A Division of Columbia Broadcasting System, Inc.
Stamford, Connecticut

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INTRODUCTION

This report covers the work completed on project No. SF 007-01-01, task 7131. The report provides an all-inclusive review of the project. It thus contains much of the information contained in the previous monthly reports, in addition to a description of the work performed since the last report and a summary.

Also included in this report is a description of the scope of the project, a description of the toristor and its possible operating modes, block diagram and circuit data sheets of the transistorized circuits designed for this project and recommendations for improving the operation of the system.

SCOPE OF PROJECT

The object of this project was to design and develop a feasibility test model of a small, thin film digital memory. The model was to be a 4 word, 2 bits/word, nondestructive, linear select memory. Readout and write-in was to be in parallel at a clock frequency of 5 mc, and addressing was to be sequential.

The memory element to be used was the toroidal thin film Ni-Fe-Co "toristor", developed by CBS Laboratories.

The goal of the project was to determine the feasibility of using the toristor in large high speed scratch pad memory systems.

Error detection circuitry was to be incorporated into the system to detect, by a bit-by-bit comparison, any descrepancy between the sensed output signal and the known storage program.

In an effort to hold the cost of the project down, those circuit functions which, though necessary for the feasibility model, would normally

be supplied to the memory subsystem from a computer, were made as simple as possible. For example, addressing was sequential rather than random and the write information was supplied from a manual switch matrix rather than a programmable information source.

THE TORISTOR

The toristor is a thin film Ni-Fe-Co cylinder which has been plated on either a glass capillary tube or a stainless steel hypodermic tube. Though its switching characteristics are similar to the planar dot memory element, it offers the following advantages:

1. A much larger output signal;
2. Nondestructive read characteristic;
3. Relative freedom from the destructive effect of strong magnetic field.

The easy direction of magnetization in the toristor is circumferentially around the rod, and in this direction the B-H hysteresis loop is square. In the hard or axial direction, the B-H loop is linear until the saturation point is reached. As with the planar film, switching is accomplished by rotation of the magnetic vector from the easy to the hard direction. Rotation from the circumferential or long direction to the axial or hard direction is accomplished by passing a current pulse through a solenoid which is wound over the toristor. Rotation of the magnetic vector appears to the sense line as a collapsing magnetic field; and therefore induces a signal on it. The polarity of the induced signal is determined by the initial direction of magnetization, i.e. whether the initial magnetization is clockwise or counter-clockwise about the sense line.

The reasons for the afore-mentioned advantages of the toroidal memory element over the planar dot are apparent when one considers the factors which

influence the magnitude of the sensed output signal. The first of these factors and the one in which the advantage of the toroidal geometry is most obvious, is the percentage of the film's total magnetic flux which is actually coupled by the sense line. Unity coupling is inherent with the toroidal configuration and is impossible in the planar configuration.

A second factor, where the advantage of the toroid is even more important but less apparent, is in the amount of magnetic flux available to be sensed. The total flux in a thin film is to a first degree approximation directly related to the cross sectional area of the film. There are, however, at least three factors which influence the maximum thickness and hence cross sectional area of the film. The first of these is that for high speed switching of the magnetization direction, it is necessary to minimize the losses due to eddy currents. Secondly, as the film thickness is increased, a point will be reached at which the film will start to switch by non-inherent rather than uniform rotation. These two factors apply equally to the toroidal and planar geometry. However, there is a third limiting factor which is unique to the planar film. At the edge of the planar film there are free magnetic poles which cause a demagnetizing field. The next result of this field is to impose a limit on the film dot size to thickness ratio; i.e., the thickness of the film may be increased only if the dot size is also increased. For a reasonable element density in a planar memory, the film thickness is limited to approximately 3000 Å.

In the toroidal configuration, this third limitation does not occur. The film is a closed loop, there are no free poles and therefore no demagnetizing fields. This permits a much greater film thickness, the toristor is typically 30,000 Å, and a correspondingly larger output signal.

In essence, the nondestructive property of the toristor is a result of its large output signal. Unlike the bicore memory, it is not an intrinsic

property of the film. If during readout of a film, the magnetization vector is not rotated to saturation in the hard direction, the vector will, upon removal of the read current pulse, rotate back to its original direction. The memory element is therefore nondestructive under low read drive conditions. This is theoretically possible with both toroidal and planar films.

Even under low read drive conditions, the toristor provides a useable output signal, upwards of 30 millivolts. The planar film, however, which even under normal read drive conditions has an output signal of only 5 to 10 millivolts, cannot tolerate a reduction in this signal and is therefore seldom operated in a nondestructive mode.

Before proceeding to a discussion of the possible operating modes of the toristor in a memory system, two other factors must be mentioned. The first of these is the fact that although the toristor is normally switched by rotation, it is possible to switch by block wall movement by applying a current of greater than H_c through the center of the toroid. When switching occurs in this manner it is slow, requiring approximately a microsecond. Finally, the sensed output signal (e) is given by the following equation:

$$e = k \tan \theta \frac{dI}{dt}$$

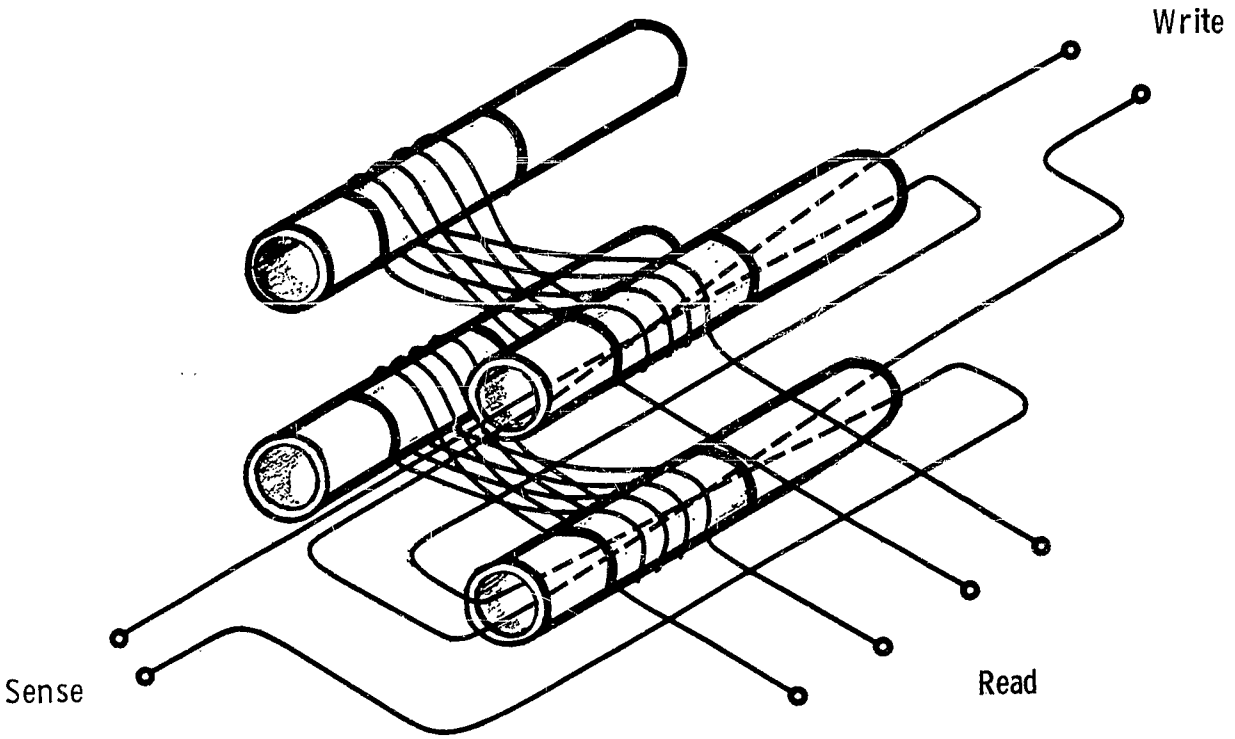
where: e = sensed output signal

θ = angle through which the magnetization vector has been rotated from the circumferential direction

I = current in the word read coil

k = constant.

The simplest mode of operation, and the mode which is used on this project, is coincident current operation. Readout is accomplished by applying a nondestructive read pulse to the work solenoid (see Fig. 1). This current rotates the magnetic vector from the circumferential direction toward the axial



MATRIX WIRING DIAGRAM

Fig. 1

direction. As was previously mentioned, the changing flux induces a voltage in the sense line and the polarity of this voltage depends on the initial direction of magnetization. Removal of the read current pulse allows the magnetic field to return to its original state. Since a signal will also be induced on the sense line when the read current is removed, and since the polarity of this signal will be opposite to that induced when the read current is increasing, it is necessary to time strobe the sense amplifiers to discriminate between the two signals.

Write-in is accomplished by the coincident application of a current in the word coil and a current in the digit winding. In the absence of other fields, the word current must be large enough to saturate the film in the hard direction. The digit current should be as large as possible but it must not produce a field greater than H_c, and it should be positioned in time such that it is at some point coincident with the word current but so that it terminates after the termination of the word pulse.

The word pulse rotates the magnetization vector to the axial direction. Then digit pulse, depending upon its polarity, rotates the vector through an additional angle into the clockwise or counter-clockwise direction. Removal of the word pulse then allows the rotation to continue to the circumferential direction.

This method of operation, though simple in concept, does have its disadvantages. The foremost of these is the need for separate word-read and word-write drivers. Some of the newer, high speed high current transistors now becoming available, may make practical the use of a second mode of operation which will eliminate the need for separate read-write drivers and thus greatly reduce the electronic circuit complexity. In this second mode of operation, write-in is accomplished by the coincidence of the nondestructive read pulse

and a digit pulse two to three times greater than H_c, but of very short duration. This method of operation depends upon the fact that if the digit pulse is short enough, the film will not switch by wall movement even though H_c is exceeded. However, the film will switch by rotation when the word current is coincidently applied. Typically, the digit current may equal 2 H_c if the pulse width is less than 50 ns and 3 H_c if it is less than 25 ns.

With this second mode of operation, the digit current should be equal to 3 H_c to assure positive write in. If it is less than 3 but greater than 2 H_c, the pulses may have to be applied a number of times before full write-in is achieved.

The advantage of the toristor relative to the planar thin film memory have been noted. There are also some disadvantages which must be noted.

The first of these disadvantages is cost per bit of storage. The planar memory's exclusive use of printed wiring reduces the cost of plane fabrication to the minimum. Although it is believed possible to automate the fabrciation of the word coils for the toristor memory, it is unlikely that the price of a toristor memory will even be less than that of the planar memory.

The second advantage of the planar memory is that the printed circuit wiring permits very accurate lead placement relative to the axis of the film and good inductive noise cancellation. The additional noise which may occur in the toristor memory is not too important because the signal is large. In most cases, the signal-to-noise ratio in the toristor memory will be better than in a planar memory of comparable size. The placement of the axis of the word coil relative to the axis of the toristor however can be crucial. Misalignment will cause the film to be easier to write-in one direction than the other and in some cases the film will spontaneously assume the preferred direction of write-in. If the misalignment is extreme, it will be impossible to write in one direction.

The toristors used in this project have been plated on stainless steel hypodermic tubing. The typical digit current for coincident current write-in is 130 ma, and H_c corresponds to a dc digit current of 150 ma. The word current for nondestructive read-in 130 ma into a 10 turn coil, and the word current for write-in is 600 ma.

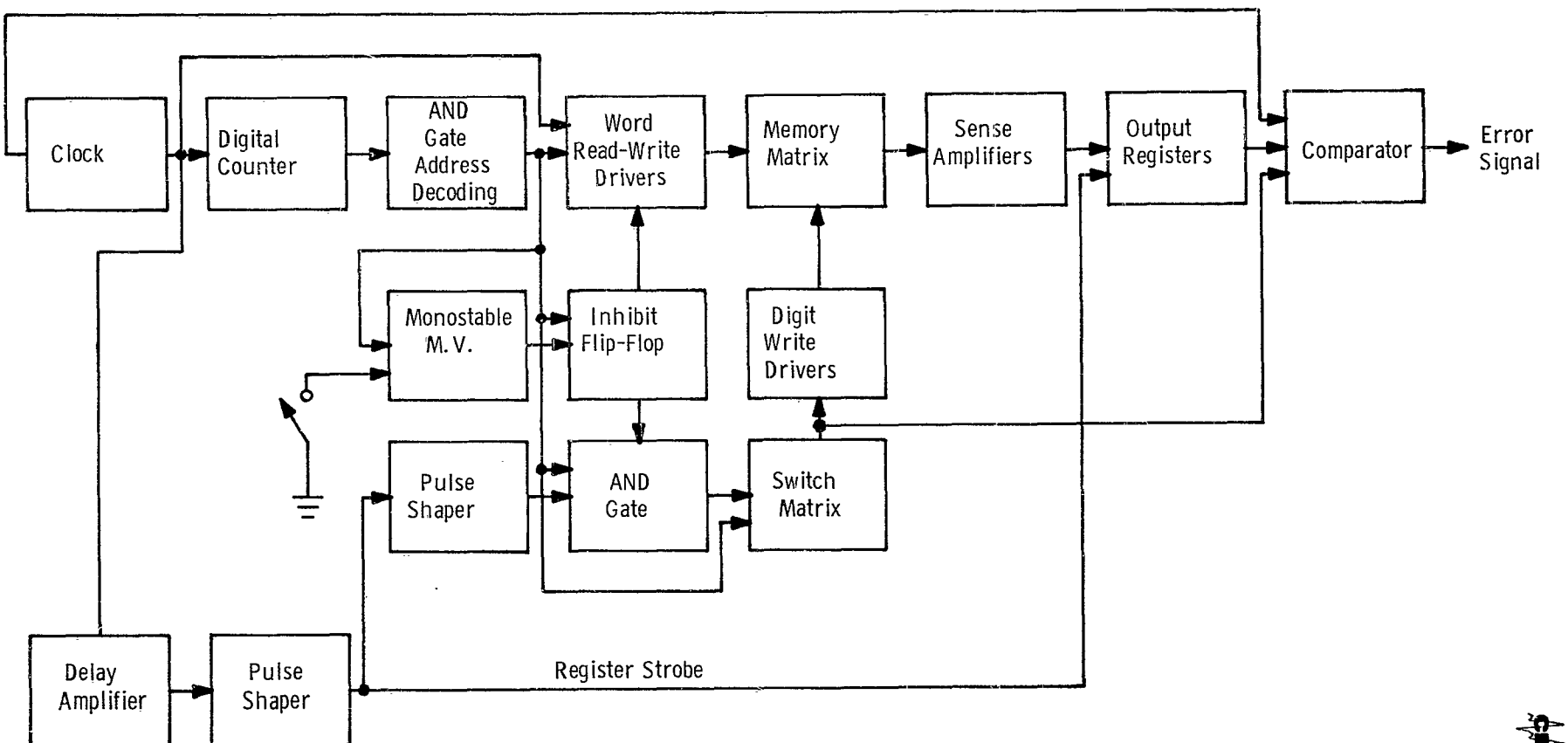
SYSTEM DESCRIPTION

The electronic system block diagram is shown in Fig. 2. The individual circuit data sheets and schematics are attached to this report. The following is a brief description of the system operation.

Sequential word addressing is achieved as follows: Sync clock pulses trigger a two stage serial counter. Address information stored in this counter is then decoded by four AND gates, and only one of which will be enabled at any one time. Coincidence of an address signal and the clock pulse, trigger one of the read current drivers.

In the initial proposal for this system, it was assumed that it would be necessary to use a parallel entry type of counter to minimize the propagation delay time of the address signal and that it would also be necessary to delay the pulse which strobes the "read drivers". It is evident that these features will be required for a larger system. However, for the small model which is the subject of this contract, the counters propagation time is insignificant and the normal propagation and rise-time delays of the "read drive" circuits are sufficient to prevent erroneous "read current" signals from occurring during the transient addressing time.

Read-out of the memory is in parallel to two differential sense amplifiers. The two outputs of each amplifier are connected in set-reset fashion to the output register flip-flops. A strobe pulse is applied to the register to prevent triggering except during the first part of the read pulse.



System Block Diagram

Fig. 2

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The differential type sense amplifier is used because of its ability to cancel common mode noise signals; i.e., signals which are capacitively coupled onto the sense line.

The register strobe pulse is derived from a delayed clock signal and a monostable multivibrator pulse shaper. The pulse is made to start slightly after the start of the word read pulse and to terminate before the end of the read pulse.

Register strobing is necessary to discriminate between the second signals which occur at the rising and falling edge of the read pulse. Comparison of the information stored in the output register with that set up by the switch matrix is made by an EXCLUSIVE-OR circuit. It is also necessary to strobe the comparator to prevent erroneous error signals from being generated during the transient times of the register and address circuits. This strobe signal may be obtained directly from the clock by arranging for the comparator and word read strobe to be 180° out of phase.

In addition to the sense lines, there are two digit write lines through the center of the toristor. Digit drives are connected to these lines so that the current produced by the two drivers passes in opposite directions through the toristor. Thus, a bipolar current is available for write-in. Selection of the proper digit driver is made via the switch matrix. Driving the write-select portion of the switch matrix are four AND gates. The gates require a signal from the inhibit flip-flop, a word address signal and a strobe pulse. Coincidence of these three pulses will activate a digit driven at each of the separate bit levels of the memory. The strobe pulse is derived from a second monostable multivibrator pulse shaper. This pulse determines the pulse width of the digit current and it is adjusted so that the digit current will terminate after the end of the word write current. The inhibit flip-flop prevents the

memory from being repetitively written.

To make certain that the program established by the switch matrix is written only once, it is necessary to activate the bit write drivers for but one complete scan of the memory address. The time duration of the enabling signal is achieved in the following manner: Coincidence of the closure of the "write switch" and address selection of word number four triggers a monostable multivibrator having a time duration greater than that required for one address scan, but less than that required for two. During this interval, word address "1" will be selected twice. The first time word "1" is selected, the inhibit flip-flop will be triggered. This in turn applies an enabling signal to the word and digit write drivers. The second time word "1" is selected, the flip-flop is again triggered, thus reapplying the inhibit signal. The pulse from the monostable multivibrator will have terminated by the time that word "1" is selected for the third time. Thus, the write operation will stop and the system will operate in the nondestructive read mode.

SYSTEM OPERATION

The major question to be answered by this contract was whether or not the toristor could operate successfully as a high speed digital memory element. This question can now be answered in the affirmative, despite the fact that some circuit modifications are still necessary in order to bring the system's performance fully up to expectations.

The system has been operated in the "read only" mode at frequencies up to 5 mc. On the following pages are oscilloscope pictures at various points in the system when operating as a scratch pad memory at a frequency of 2.5 mc.

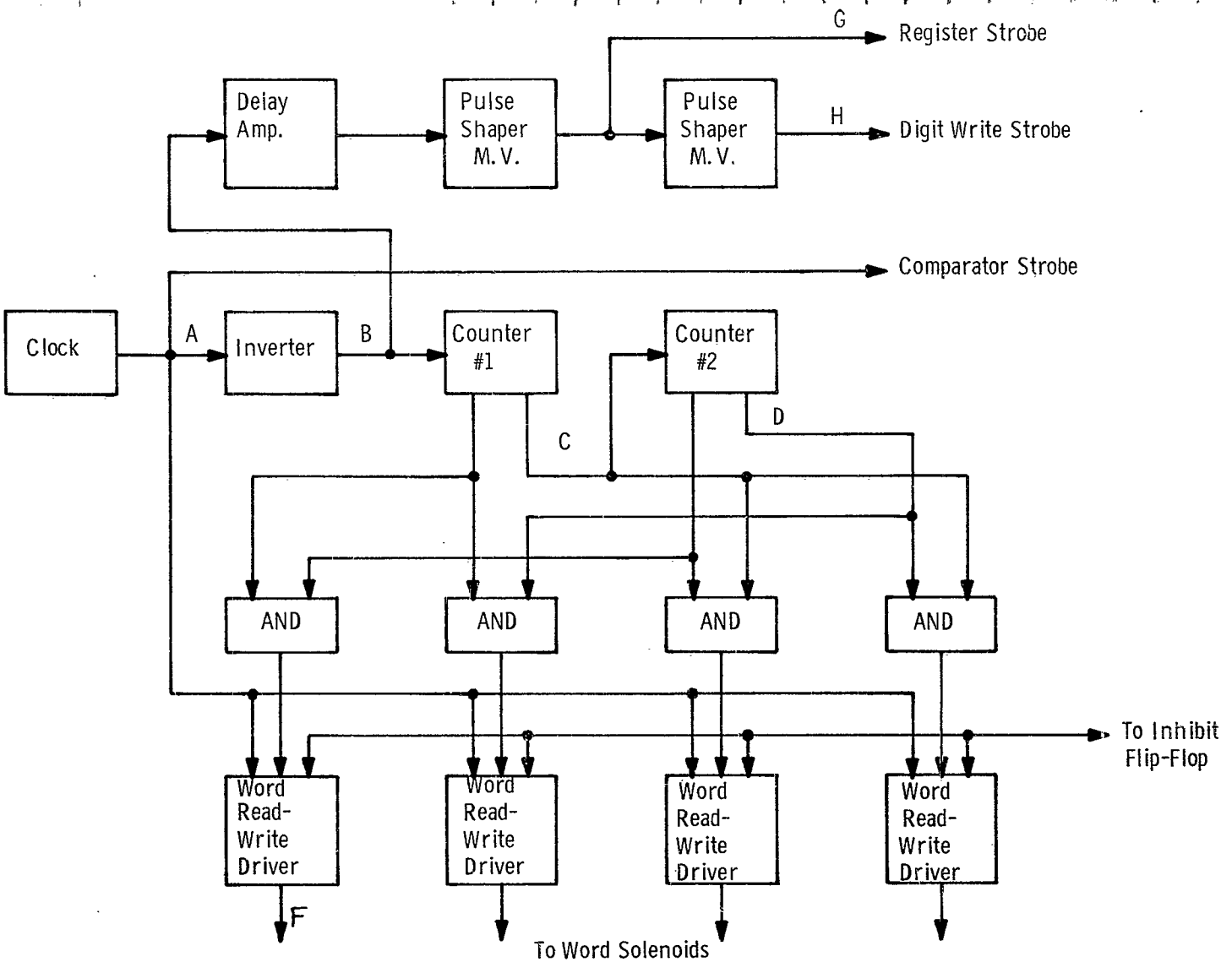
These photographs are referenced to the detailed block diagrams (Figs. 3, 4 and 5) by the letter in parenthesis at the side of each waveform. When these photographs were taken, one word was not operational (see Fig. 8).

Most of the waveforms of interest are shown in Figs. 6, 7 and 8. The single transient signals in the write circuitry are omitted, i.e. the inhibit signal, where it was difficult to obtain sufficient time intensity to photograph. The word and digit write signals were photographed by temporarily removing the inhibit signal.

Most of these waveforms and their phase relationships have been described elsewhere. By way of repetition, however, it should be noted that although a signal may be sensed at the trailing edge of the read pulse, its position in time is such that the register strobe will discriminate against it (Fig. 8). Also of special importance is the position of the "digit write" relative to the "word write" pulse (Fig. 7). The digit pulse must read a maximum while the word pulse is also at its maximum level, and must fall only after the read pulse has ended. Fig. 9 illustrates the timing of the clock, two counters, "AND" gates and inhibit flip-flop, photographs of which are shown in Fig. 6.

CONCLUSIONS

The system, were it to be evaluated only upon the three operating words and one bit level shown by these photographs, would be given unqualified approval. The system is operating at a cycle time approximately five to ten times faster than is possible with ferrite cores. With proper readjustment of the clock frequency and timing network, the cycle time might easily be increased by a factor of two. Write-in is achieved by a single coincidence of the "word write" and digit currents and there is perfect detection of the signal caused by the rise of the read pulse and rejection of the signal caused



Detailed Block Diagram

Fig. 3

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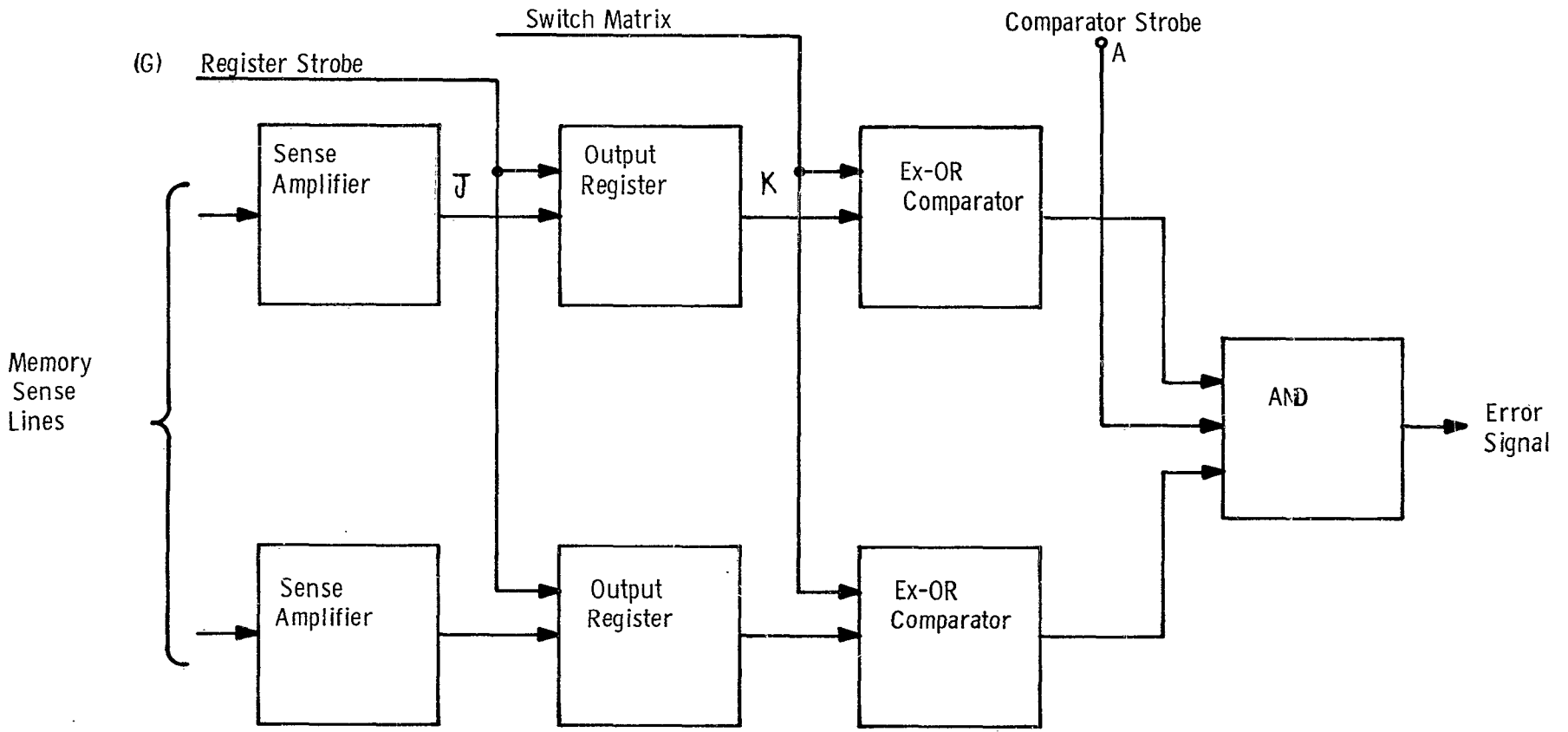

Detailed Block Diagram

Fig. 4

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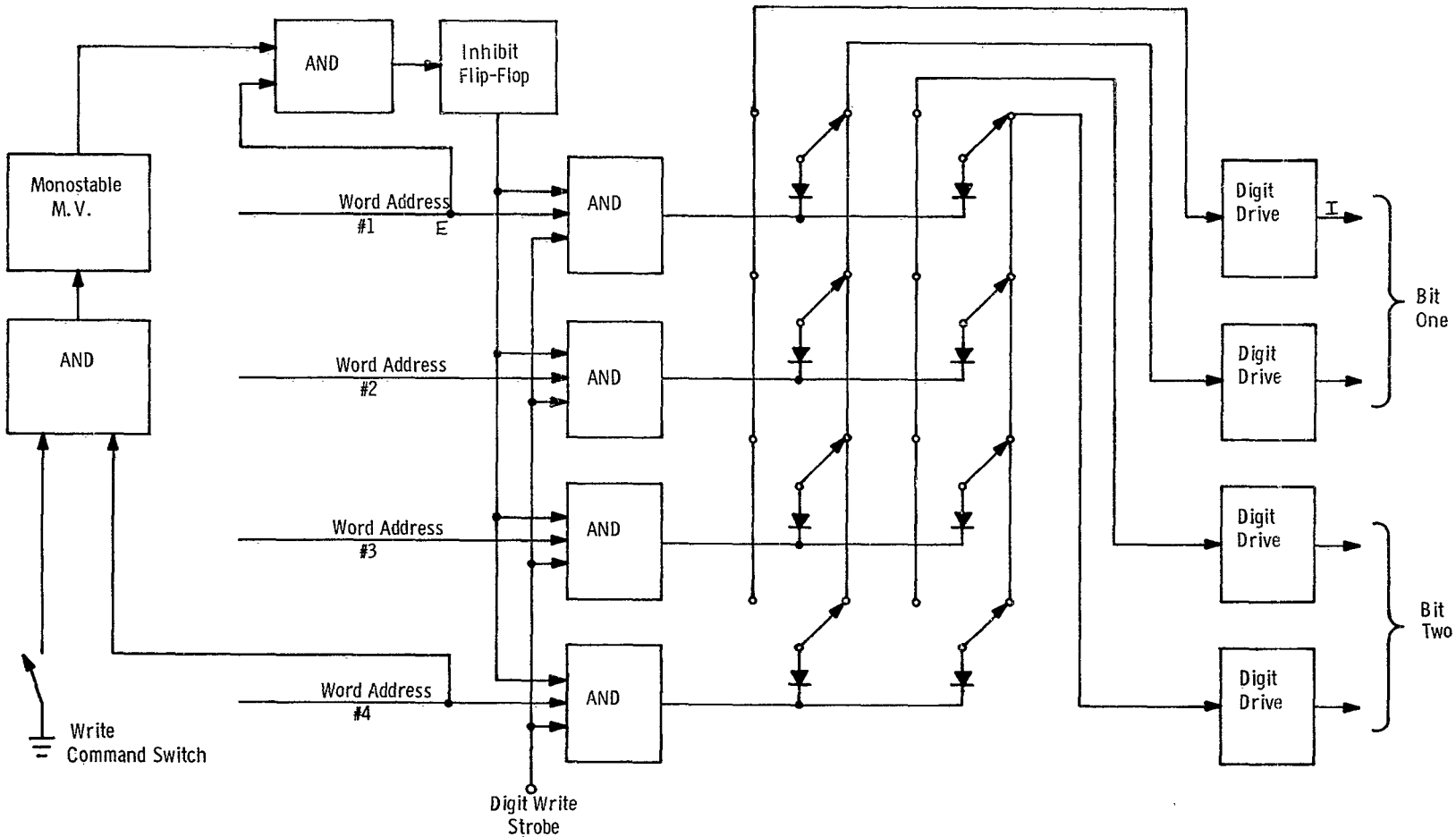
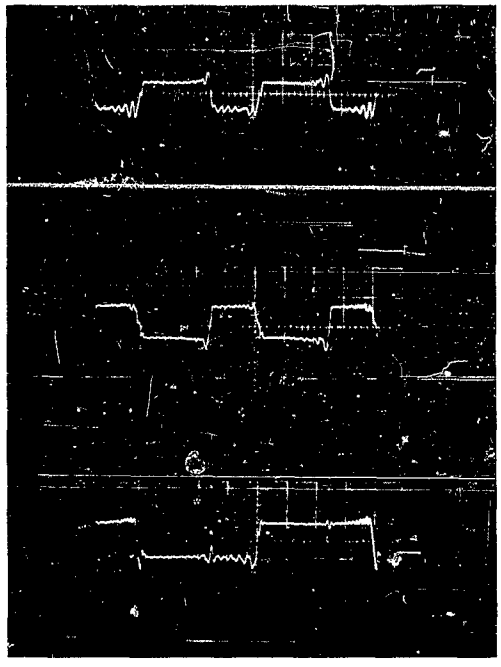


Detailed Block Diagram
Fig. 5

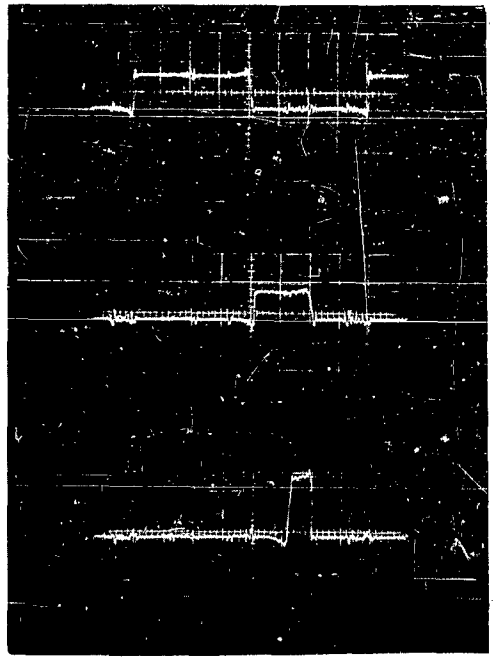
CBS LABORATORIES



(A) Clock output
5 volts/cm 100 ns/cm

(B) Input to 1st counter
5 volts/cm 100 ns/cm

(C) Output at 1st counter
5 volts/cm 100 ns/cm

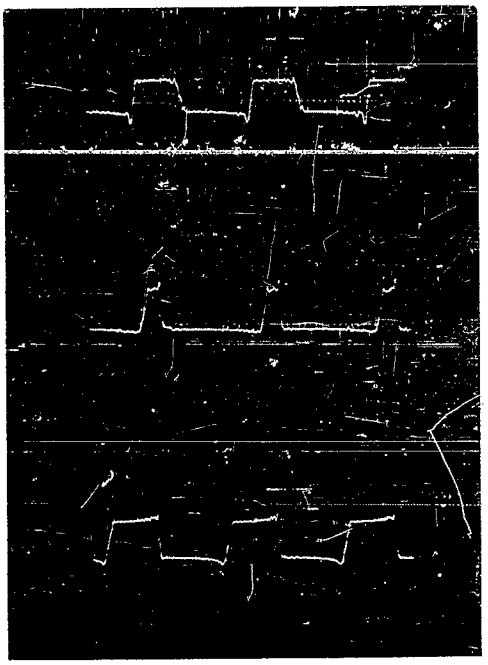


(D) Output at 2nd counter
5 volts/cm 200 ns/cm

(E) Output at word #1 address decoding gate
5 volts/cm 200 ns/cm

(F) Word #1 read current pulse
60 Ma/cm 200 ns/cm

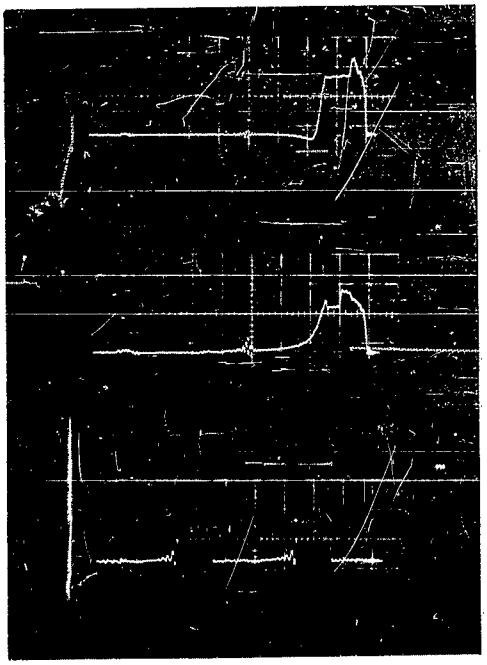
FIGURE 6



(B) Output of Inverter
5 volts/cm 100 ns/cm

(G) Output Register Strobe
5 volts/cm 100 ns/cm

(H) Digit Write Strobe
5 volts/cm 100 ns/cm

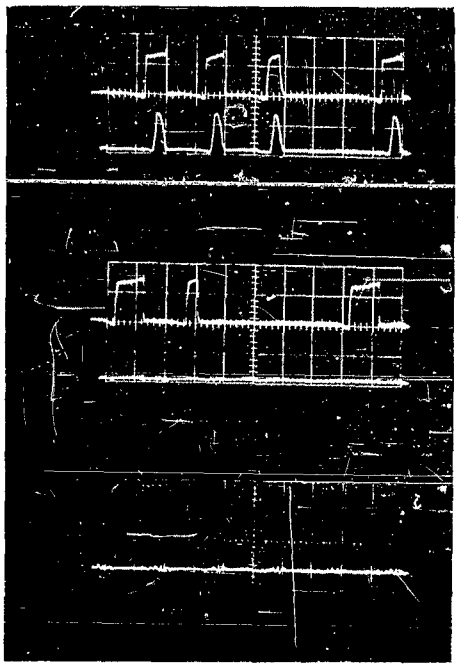


(F) Word #1 Read Pulse
60 Ma/cm 100 ns/cm

(F) Word #1 Write Pulse
Approx. 300 Ma/cm 100 ns/cm

(I) Digit Write Current Pulse
60 Ma/cm 100 ns/cm

FIGURE 7



(J) Sense amplifier output (Side "1")
5 volts/cm 200 ns/cm

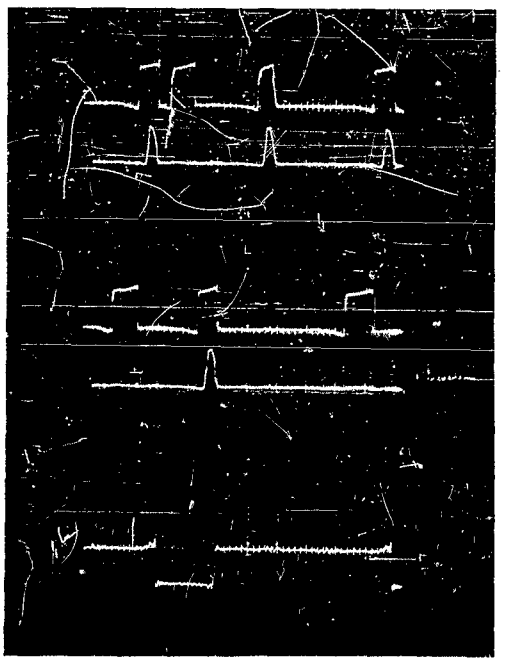
Strobed sense signal
5 volts/cm 200 ns/cm

Sense amplifiers output (Side "0")
5 volts/cm 200 ns/cm

Strobed sense signal
5 volts/cm 200 ns/cm

(K) Register output

In the above photograph the stored information is -,1,1,1



(J)

The waveforms are the same as those above except that the stored program is -,1,0,1

(K)

FIGURE 8

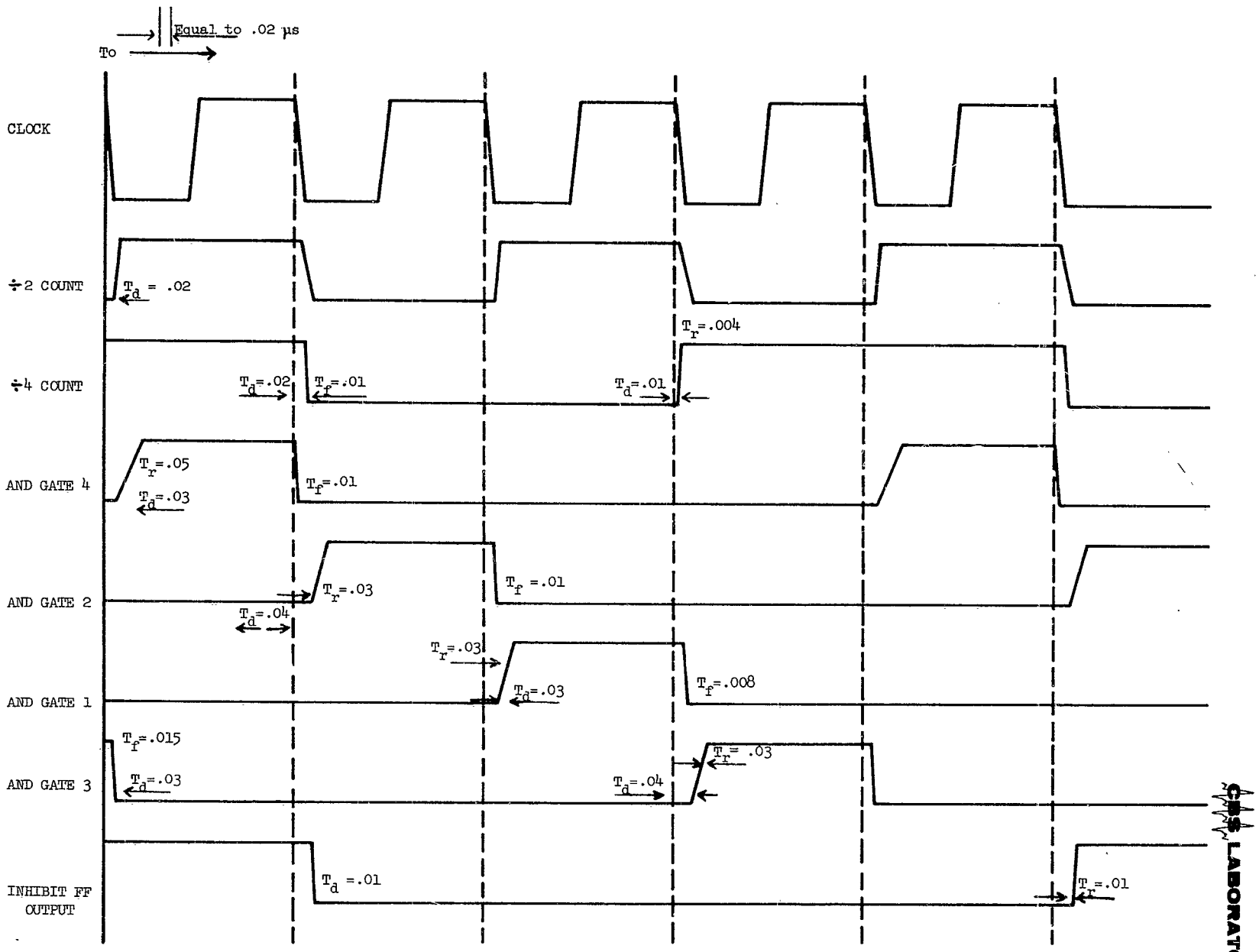


FIG. 9 TIMING DIAGRAM

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by the fall of the read pulse.

Unfortunately, Fig. 8 shows what is possible and not what is invariably obtained. It represents the system when it is on its best behavior, when the word coils are accurately positioned and tightly coupled to the toristor rod. This marginal performance is indirectly but inescapably caused by the "word write" driver, the circuit which was of so much concern in previous monthly reports. This problem is particularly disturbing because reliable read-out is not in, and of itself, difficult to achieve.

During the early part of the development, when the breadboard was operating in the "read only" mode, the same circuit that is now the digit driver was also used as the "word read" drive. With this stage, no serious read out difficulties were encountered. Recalling the equation relating to output signal voltage and drive current ($e = k \tan \theta \, di/dt$) and examining the difference between the wave shape of the digit current pulse and the read pulse currently being used (see Fig. 7), reveals some of the reasons for the problems which have been encountered. The rise time of the read pulse is relatively slow, and di/dt is especially slow at high current levels where the factor $\tan \theta$ is most important. The net result is a decreased signal amplitude and a detection problem.

The write driver enters the picture because it was to accommodate it, that compromises were made in the read driver. It is believed that most of the difficulties now being encountered would be eliminated if the original read driver design were used, i.e. the digit driver circuit, and if a "write driver" were designed using a high current low saturation time transistor (National Semiconductor 2N2403) to operate in the saturated mode. This was the original intention, but when a six month delivery date was quoted on the 2N2403, it became necessary to find a substitute power output transistor. The substitute had to operate in a nonsaturated state for high frequency operation

and, since the "read" and "write" drivers drive a common point, it was in turn necessary to redesign the "read drivers".

The inhibit flip-flop circuit should be revised to reduce its sensitivity to noise. At present, this circuit tends to turn ON and cause destruction of "word drive" transistors and coil windings, if the circuit is not under constant surveillance. One recommendation would be the use of a monostable multivibrator whose period is equal to one "word cycle".

In addition, a more thorough review of the sense amplifier is warranted to determine its noise rejection ratio.

In general, it is believed that additional reliability, even in this breadboard model, could be assured by repackaging the circuitry in a form which would be less noise sensitive.

As a summary of this section, it can be stated that the toristor is a usable digital storage device for operation in a "nondestructive read" mode to frequencies of 5 mc, and as a scratch pad memory to 2.5 mc. It has been so operated. Though the system in its present state of design is marginal, it has been shown that this is not caused by any basic fault in the toristor, but rather indicates the need for redesign of the word "read-write" driver.

Despite this proof of feasibility, which comes after considerable CBS investment both in the original development of the toristor by G. V. Planar, Ltd. under contract to CBS Laboratories and during the course of this project, the promise of more immediate returns in other areas of Laboratory activities, has forced us to conclude that no further investment can be made in the toristor. Therefore, with the prime question of feasibility answered in the affirmative, it was mutually agreed by CBS Laboratories and the cognizant Bu Ships personnel that this final report be submitted.

CLOCK PULSE GENERATOR

A. Description

This circuit is an astable multivibrator stage. It differs from the conventional Eccles-Jordan configuration in two important respects. First, to improve the rise and fall time of the stage, the timing capacitors are connected to emitter followers rather than to the collectors of the multivibrator transistor. And second, the base resistor of each multivibrator transistor is connected via a diode to the collector of the opposite transistor rather than to the V_{CC} supply. The second feature assures that the stage will be self starting, for should both transistors attempt to turn on, insufficient base current can be drawn through R_3 and R_4 to maintain this condition.

B. Application

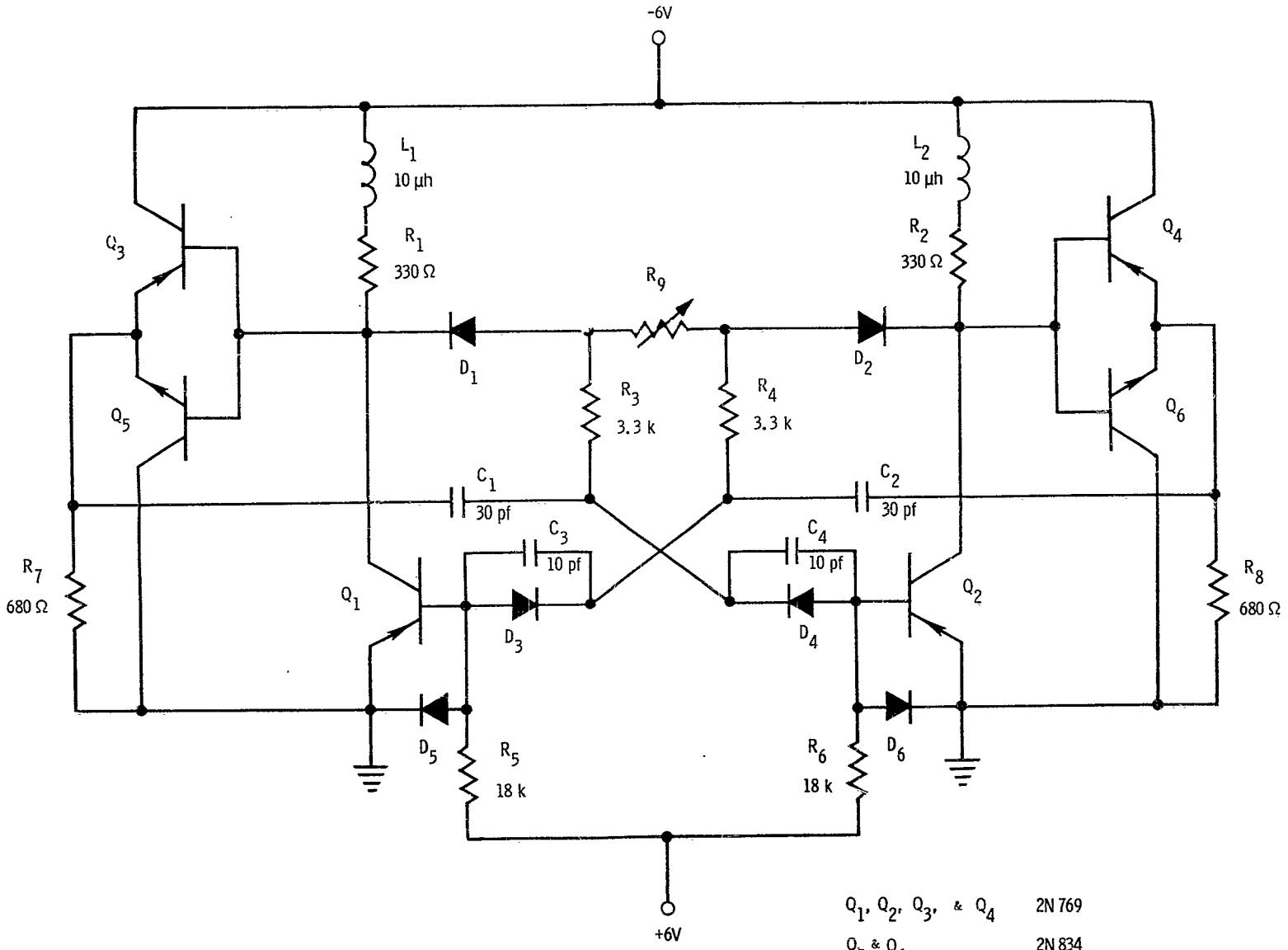
This stage is to be used for the generation of timing clock pulses.

C. Circuit Schematic

See Figure 10

D. Specifications

1.	Output	6 volts clamped to ground and -6 volts typical rise time 10 ns typical fall time 10 ns
2.	Frequency	Variable with R_9, and C_1 and C_2 f = 5 mc when R_9 = 0, C_1 = C_2 = 30 pf
3.	Power Requirements	-6 volts, 30 ma +6 volts, 0.7 ma



Q_1, Q_2, Q_3, & Q_4	2N 769
Q_5 & Q_6	2N 834
All diodes	1N 914

FIG. 10

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20 MC COUNTER

A. Description

This circuit is a bistable flip-flop counter, capable of operation at rates in excess of 20 Mc. The output of the counter is taken from an emitter-follower buffer stage, thus preventing the load from slowing the circuit operation. The output is a 6 volt signal clamped between ground and -6 volts.

B. Application

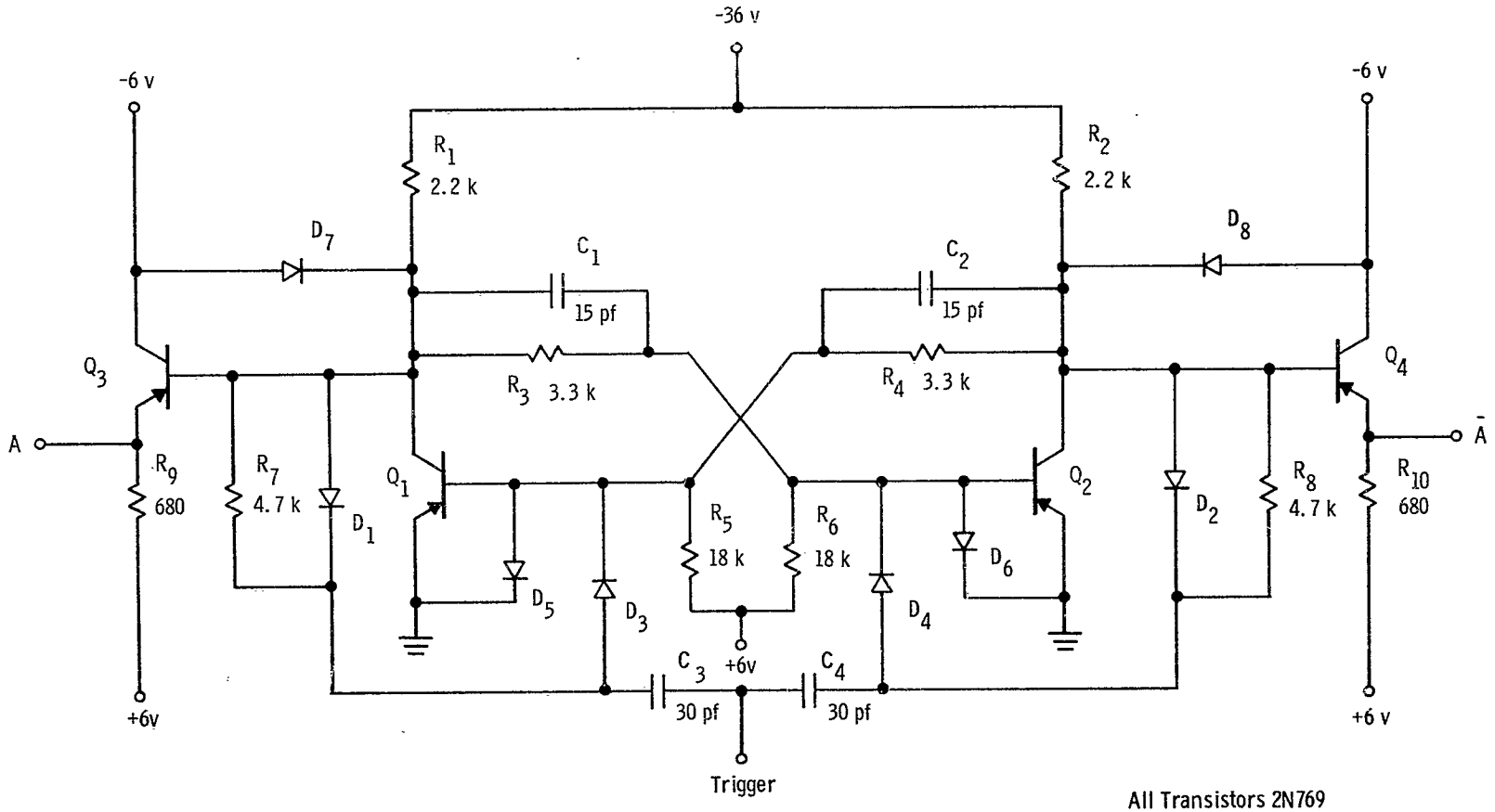
The circuit is to be used to supply the sequential addressing information for the memory system.

C. Circuit Schematic

See Figure 11

D. Specifications

1. Input	6 volt ± 10% positive pulse minimum pulse width--20 ns maximum rep-rate--20 mc
2. Output	6 volts clamped to ground and -6 volts typical delay time 6 ns typical rise time 10 ns } 25°C typical fall time 10 ns
3. Power Requirements	-36 volts, 30 ma - 6 volts, 13 ma + 6 volts, 27 ma



All Transistors 2N769
All Diodes IN914

20 MC DIGITAL COUNTER

FIG. 11

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DECODING AND GATE

A. Description

This stage consists of a positive diode AND gate followed by a complementary emitter-follower amplifier. The circuit is designed to drive a 35 ma, 6 volt signal into a resistive load at a maximum rep-rate of 20 mc.

B. Application

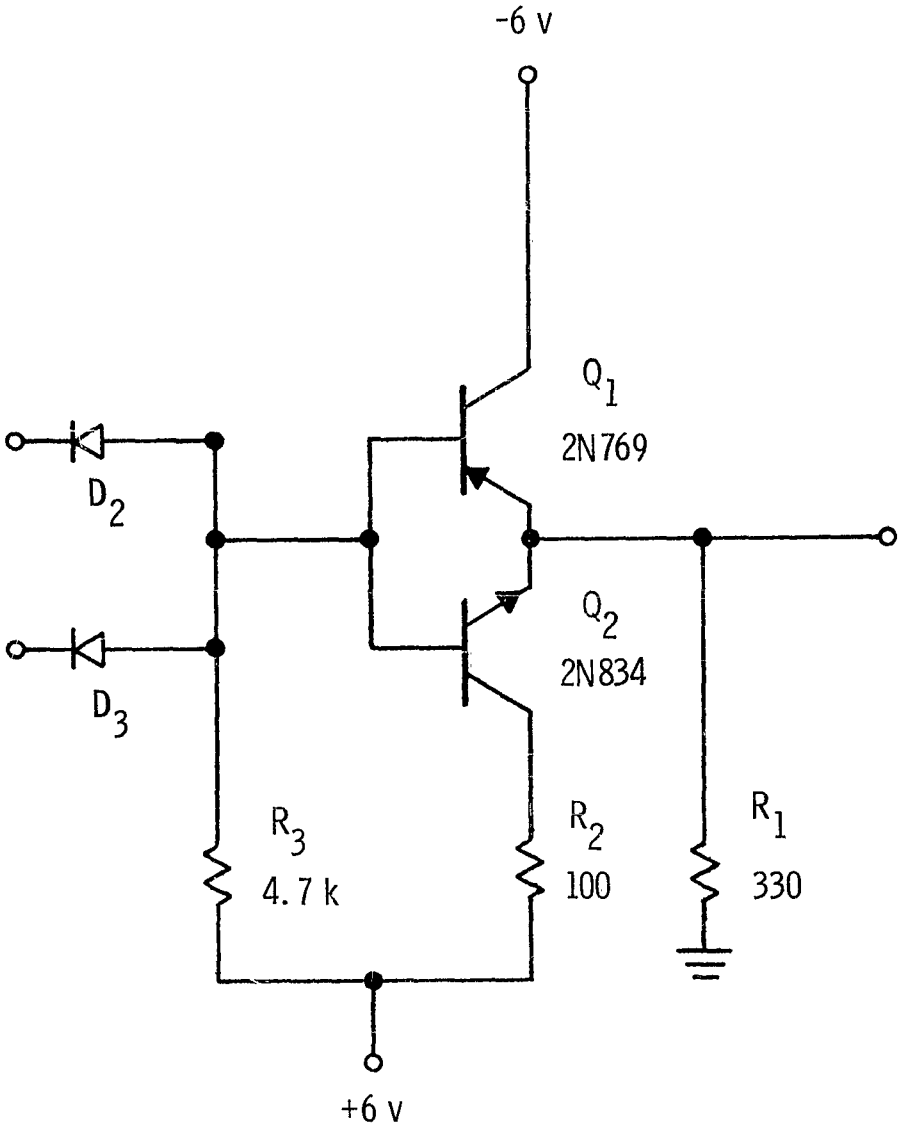
The circuit is to be used for the word address decoding. The output will drive the switch matrix and the inputs to the word read and write drivers.

C. Circuit Schematic

See Figure 12

D. Specifications

1. Input	6 volts clamped between ground and - 6 volts. Inhibit current--4.5 ma max.	
2. Output	Source or sink for a maximum 35 ma resistive load. Output waveform follows input.	
3. Power Requirements	-6 volts +6 volts	} Current varies with load



All Diodes 1N914

AND GATE DECODING AMPLIFIER

Fig. 12

SENSE AMPLIFIER

A. Description

The sense amplifier is designed to amplify a 20 mv input signal, and produce a 6 volt output pulse. The input stage is a differential amplifier which not only amplifies the input signal but also tends to cancel any common-mode signal, i.e. any capacitively coupled signal, that may be on the input line. A common-emitter stage, operated class A, is connected to each of the outputs of the differential amplifier stage. These circuits in turn drive a digital inverter stage which has its output clamped to ground and -6 volts. Depending on whether the input signal is positive or negative, an output signal will be obtained at either the "1" or the "0" terminal.

B. Application

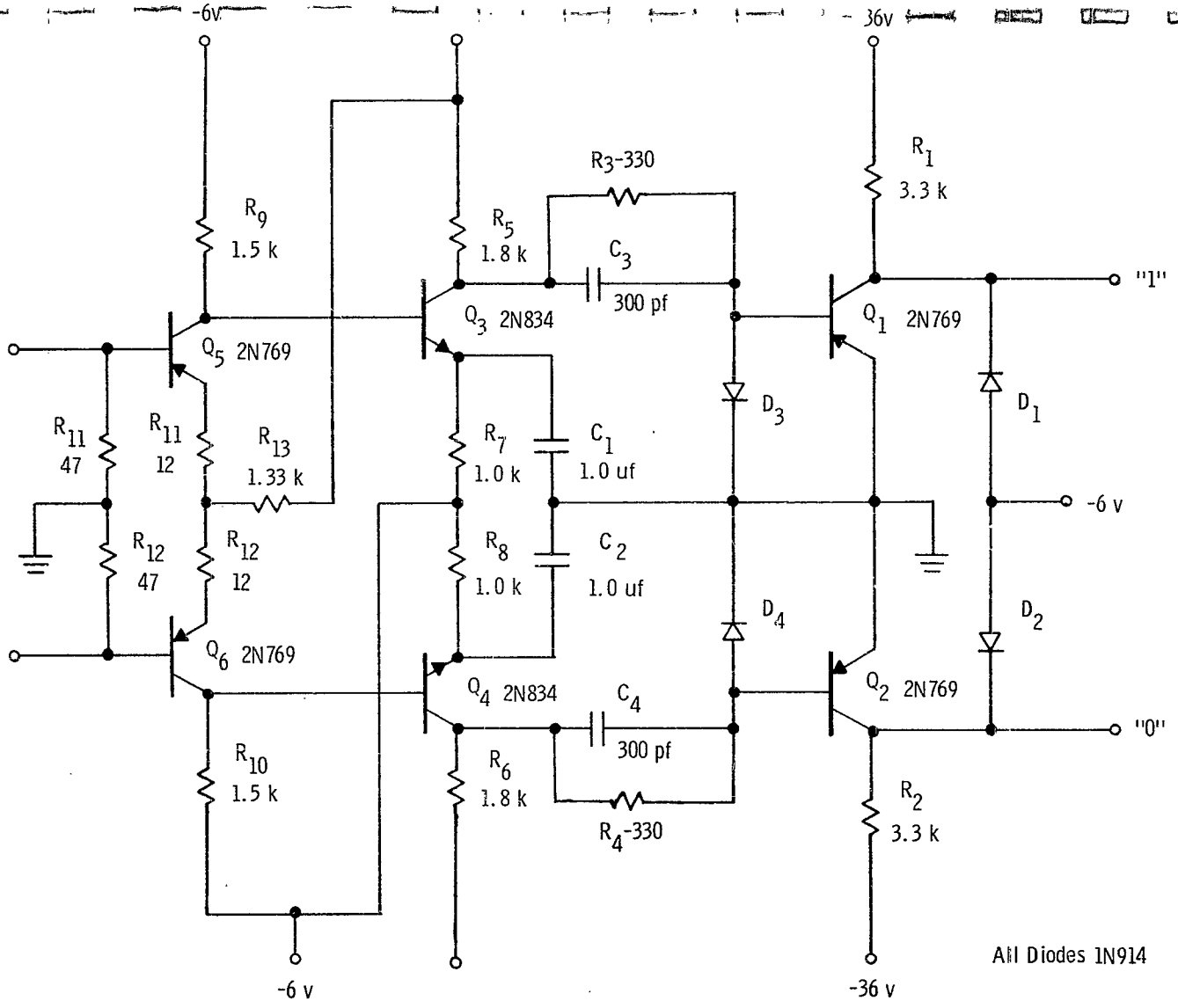
Sense amplifier.

C. Circuit Schematic

See Figure 13.

D. Specifications

1.	Input	Greater than $\pm$ 20 mv.
2.	Output	6 volts, clamped to ground and -6 volts.
3.	Power Requirements	-36 volts, 20 ma (peak) - 6 volts, 8 ma + 6 volts, 10.5 ma



SENSE AMPLIFIER

Fig. 13

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OUTPUT REGISTER

A. Description

This circuit is a bistable flip-flop which uses the set-reset mode of triggering. Triggering is accomplished via an AND gated emitter-follower. The emitter-follower prevents the capacitors C_3 and C_4 from loading the previous stages, and the AND gate permits time strobing of the trigger pulse received from the sense amplifiers. The output signal is clamped between ground and -6 volts, and the maximum frequency of operation is in excess of 10 mc.

B. Application

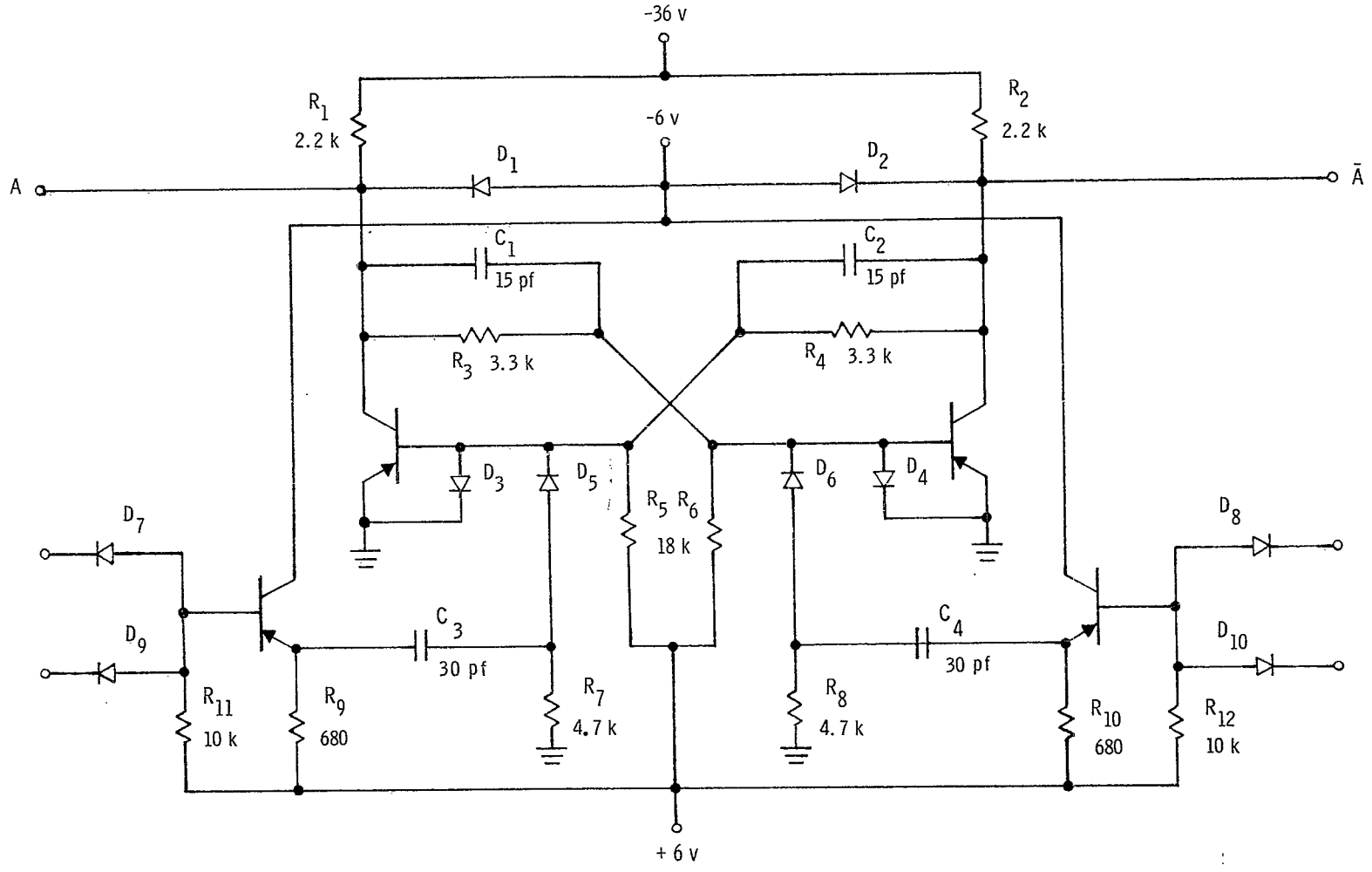
The stage is to be used for buffer storage of the information received from the sense amplifiers.

C. Circuit Schematic

See Figure 14.

D. Specifications

1. Input	6 volts clamped to ground and -6 volts inhibit current 1.35 ma max. maximum rep-rate 10 mc.
2. Output	6 volts clamped to ground and -6 volts typical rise time 10 ns typical fall time 10 ns
3. Power Requirements	-36 volts, 30 ma - 6 volts, 20 ma + 6 volts, 35 ma



All Diodes 1N914
All Transistors 2N769

FIG. 14 OUTPUT REGISTER

CBS LABORATORIES

COMPARATOR

A. Description

The comparator is an EXCLUSIVE - OR circuit. The output taken from the common collector, point C, is at -6 volts when either A and B are at ground, or when $\bar{A}$ and $\bar{B}$ are at ground. Electrically the function generated is $C = (A + B) \cdot (\bar{A} + \bar{B})$ and this is equal to $(A.B) + (\bar{A} \cdot \bar{B})$.

B. Application

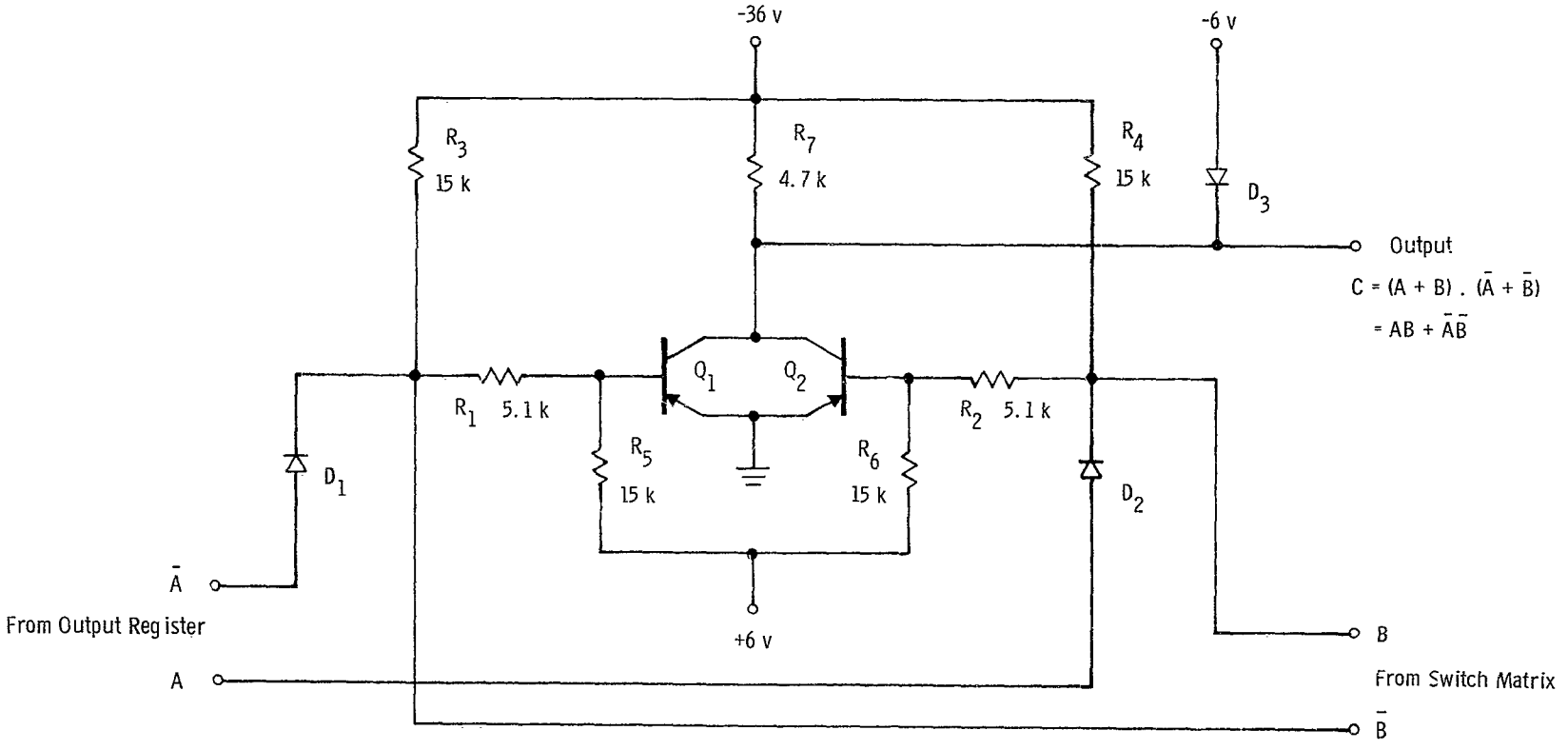
The circuit is used for error detection. It compares the information stored in the output register with the information set up by the memory switch matrix.

C. Circuit Schematic

See Figure 15.

D. Specifications

1.	Input	6 volts clamped to ground and -6 volts inhibit current 2.5 ma
2.	Output	6 volts clamped to ground and -6 volts $C = (A.B) + (\bar{A}.\bar{B})$
3.	Power Requirements	-36 volts, 12.5 ma (peak) - 6 volts, 6.5 ma + 6 volts, 1.0 ma



All Diodes 1N914
All Transistors 2N769

FIG. 15 EXCLUSIVE OR COMPARATOR

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MONOSTABLE MULTIVIBRATOR

A. Description

This stage is a conventional monostable circuit. The only feature which is at all unusual is the use of the diode D_5 in Q_2 's base circuit. This diode is used to prevent excessive reverse bias from being applied to the base-emitter junction of Q_2; and, because of the low leakage of the diode, the delay time of the stage is relatively uneffected by temperature changes.

B. Application

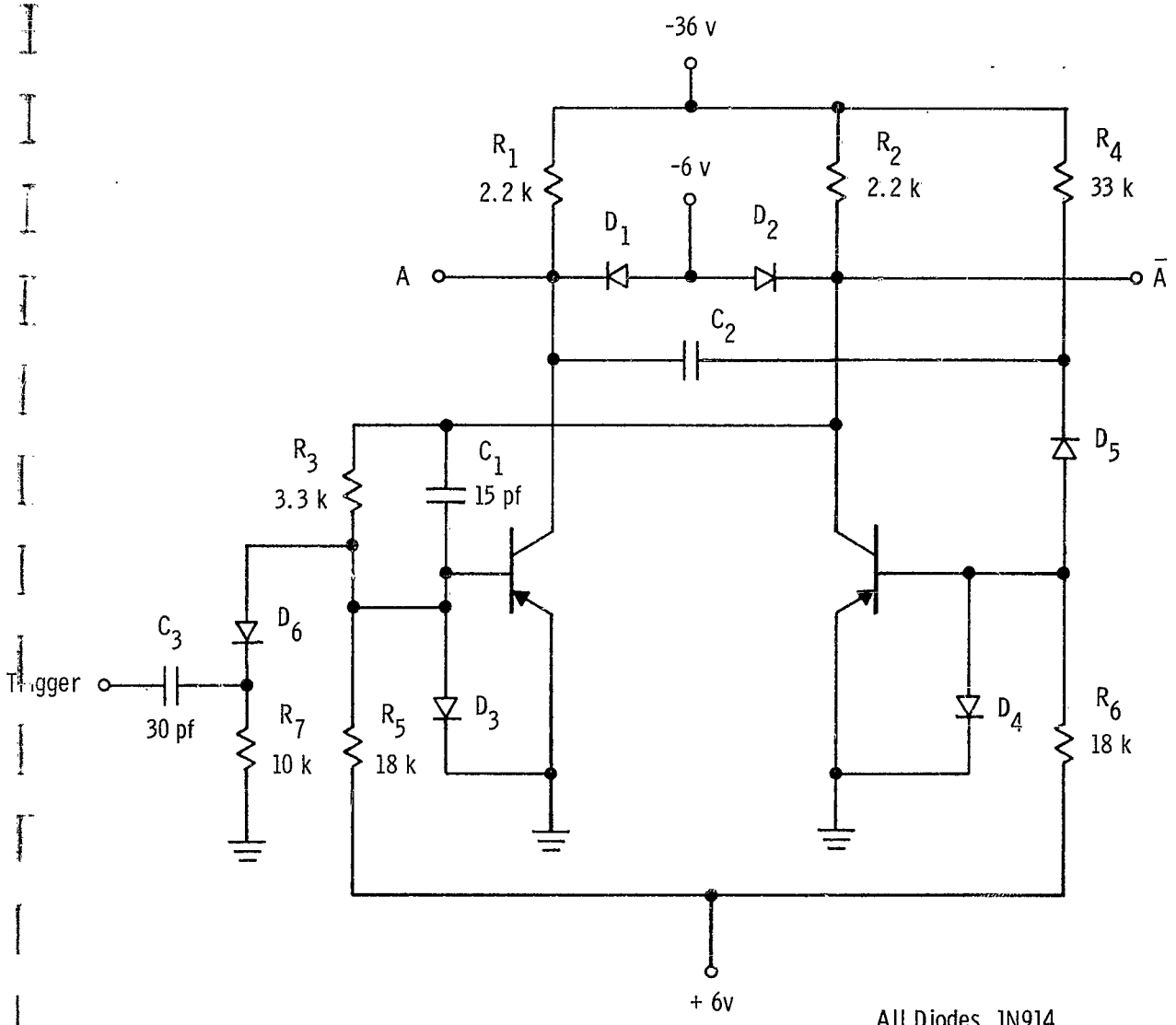
The circuit is used for the generation of a fixed time delay.

C. Circuit Schematic

See Figure 16.

D. Specifications

1. Input	6 volts positve pulse minimum pulse width 20 ns maximum rep-rate 10 mc
2. Output	6 volts clamped to ground and -6 volts delay time varies directly with C_2 typical rise time 10 ns typical fall time 10 ns
3. Power Requirements	-36 volts, 30 ma - 6 volts, 11 ma + 6 volts, 1.0 ma



All Diodes 1N914
All Transistors 2N769

MONO-STABLE MULTIVIBRATOR

Fig. 16

DIGIT WRITE DRIVER

A. Description

The read driver is designed to drive a 150 ma current pulse into the approximately 0.5 uh inductance of the word coils. The pulse rise time is less than 20 ns.

The circuit consists of a positive diode AND gate followed by a three stage common-emitter amplifier. Coincident of an address signal and the read strobe pulse results in an output signal which has a duration equal to that of the strobe.

B. Application

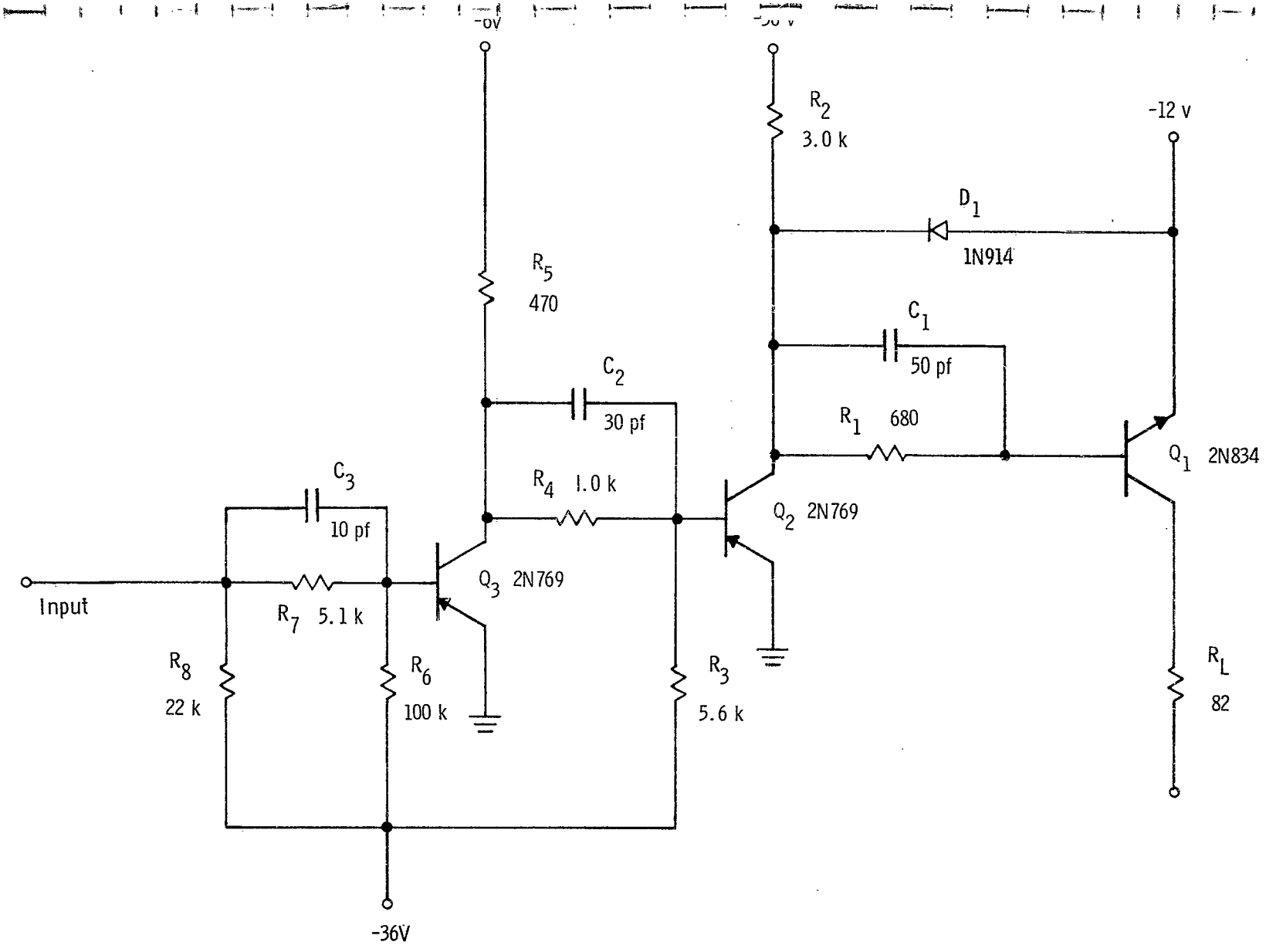
Word read drive.

C. Circuit Schematic

See Figures 17 and 18.

D. Specifications

1. Input	6 volt pulse, clamped to ground and -6 volts $t_r < 10$ ns Duty factor < 20%
2. Output	150 ma pulse pulse width equal to input $t_r < 20$ ns into 0.5 uh inductive load
3. Power Requirements	-36 volts, 12 ma (peak) -12 volts, 165 ma (peak) - 6 volts, 13 ma + 6 volts, 1.5 ma



Digit Write Driver

Fig. 17

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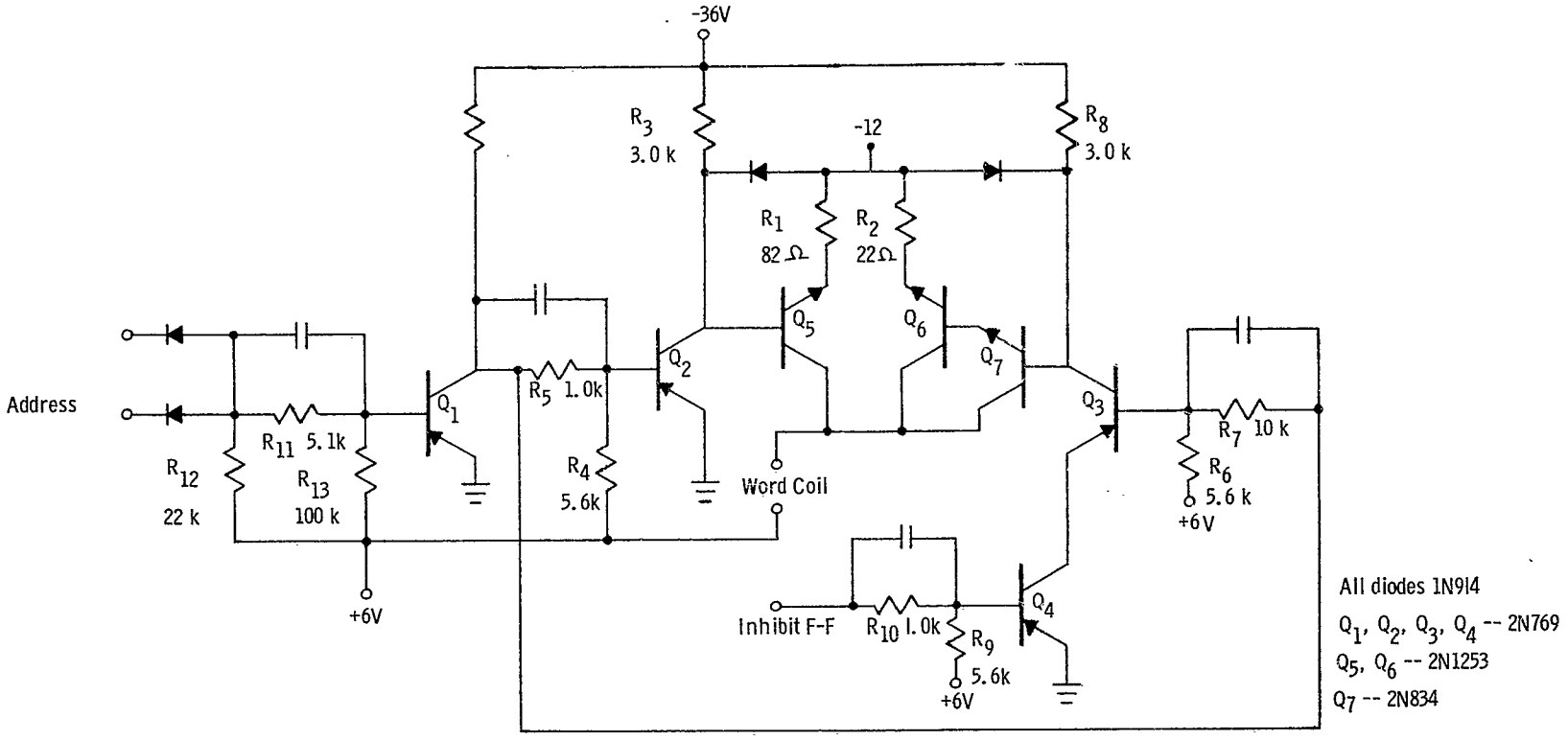

Word Read-Write Drivers

Fig. 18

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